REMARKS

Claims 1, 3 and 6-8 are pending in the instant patent application. Claims 2, 4, 5 and 9-15 were previously canceled. Applicants respectfully request reconsideration of the instant application and pending Claims.

Examiner Interview

Applicants respectfully request an Examiner's Interview prior to the issuance of the next Office Action if the next Office Action includes a rejection that is again based on the Tanaka and Heim references discussed below.

103 Rejection

Claims 1, 3 and 6-8 are rejected under 35 U.S.C. 102 as being anticipated by Tanaka (US Patent No. 6,756,675; hereinafter "Tanaka") in view of Heim (US Patent No. 5,248,903). Applicants have reviewed the cited reference and respectfully submit that the embodiments of the claimed invention that are set forth in Claims 1, 3 and 6-8 are not anticipated or rendered obvious by Tanaka in view of Heim.

The Examiner is respectfully directed to independent Claim 1 which is drawn to a semiconductor device. Claim 1 is reproduced in its entirety below for convenience of the Examiner.

1. A semiconductor device comprising:

a pad metal layer having a perimeter area and a center area;

a lower metal layer having a plurality of apertures below said center area

of said pad metal layer, wherein said apertures are arranged into a plurality of rows each row comprising more than one of said apertures and a plurality of columns each column comprising more than one of said apertures;

an interlayer dielectric formed between said pad metal layer and said lower metal layer wherein said interlayer dielectric covers a portion of both the bottom and the sides of said pad metal layer;

a plurality of vias formed in said interlayer dielectric, wherein said plurality of vias electrically couple said pad metal layer and said lower metal

layer, and wherein said plurality of vias form a ring arrangement that is located above and outside of the region occupied by said apertures in said lower metal layer and below an outermost perimeter area of said pad metal layer; and

an insulating dielectric layer that covers said perimeter area of said pad metal layer wherein said insulating dielectric layer covers a portion of both the top and the sides of said pad metal layer.

Claims 3 and 6-8 depend from Claim 1 and recite additional limitations of the claimed invention.

Tanaka in view of Heim does not anticipate or render obvious the embodiments of the invention as set forth in Claims 1, 3, 6 and 8. Tanaka in view of Heim is deficient as Tanaka does not teach or suggest all of the limitations of the claimed embodiments and Heim does not remedy the deficiencies of Tanaka. In particular, Tanaka does not teach or suggest a semiconductor device that includes an insulating dielectric layer and a plurality of vias formed in an interlayer dielectric that is formed between a pad metal layer and a lower metal layer that has apertures, "wherein said interlayer dielectric covers a portion of both the bottom and the sides of said pad metal layer" and "wherein said insulating dielectric layer covers a portion of both the top and the sides of said pad metal layer" as is recited in Claim 1 (upon which Claims 3, 6 and 8 depend). Furthermore, Heim does not teach or suggest modifying Tanaka in a manner that remedies the above noted deficiencies of Tanaka. In fact, Heim does not teach or suggest these limitations at all.

Claim 1 has been amended to delimit how the interlayer dielectric and the insulating dielectric are disposed in relation to the pad metal layer. Support for the newly added limitations can be found in Applicants' specification at page 4, lines 11-37 and in Figure 2. It is important to note that the newly added limitations describe the portions of the pad metal layer that are covered by the interlayer dielectric layer and the portion of the pad metal layer that are covered by the insulating dielectric layer. It should be appreciated that this limitation (along with the others recited in the Claims) must be taught or suggested by the cited reference in order for a proper prima

facie case for rejection to be supported thereby. However, Applicants respectfully submit that the newly added limitations are not taught or suggested anywhere by Tanaka in view of Heim. If a rejection based on Tanaka in view of Heim is maintained Applicants respectfully request that the location in the references where the aforementioned limitations are taught or suggested be identified.

Applicants understand Tanaka to disclose a semiconductor device that provides a high density connecting region arrangement that is dissimilar to the claimed embodiments of Applicants' invention. In particular, Tanaka does not teach or suggest the limitations that have to do with the disposition of the interlayer dielectric layer and the insulating dielectric layer with respect to the pad metal layer. In the outstanding Office Action protecting film 240 is equated to the recited insulating dielectric layer, insulating layer 150 is equated to the recited interlayer dielectric layer, and third electrode layer 100 is equated to the recited pad metal layer. Applicants respectfully submit that in contrast to the disposition of the recited insulating layer with respect to the recited pad metal layer delimited in Claim 1 that protecting film 240 is situated only above a portion of the third electrode and does not cover a portion of the sides of the third electrode. Moreover, in contrast to the disposition of the recited interlayer dielectric layer with respect to the recited pad metal layer delimited in Claim 1, insulating layer 150 covers only the bottom portion of the third electrode and does not cover a portion of the sides of the third electrode. Accordingly, the Claim 1 limitations drawn to the disposition of the interlayer dielectric layer and the insulating dielectric layer with respect to the pad metal layer cannot be reasonably interpreted as being met by the subject matter referenced in the outstanding Office Action related to the protecting film 240, insulating layer 150 and third electrode 100 disclosed by Tanaka.

Based on Applicants' aforementioned review of Tanaka, Applicants respectively submit that nowhere in the Tanaka reference is a semiconductor device taught or suggested that includes an insulating dielectric layer and a plurality of vias formed in an interlayer dielectric that is formed between a pad metal layer and a lower metal layer that has apertures, "wherein said interlayer dielectric covers a portion of both the bottom and the sides of said pad metal layer" and "wherein said insulating

dielectric layer covers a portion of both the top and the sides of said pad metal layer" as is recited in Claim 1 (upon which Claims 3, 6 and 8 depend). Consequently, as alluded to above, Tanaka fails to teach or suggest all of the limitations recited in Claim 1.

Heim does not teach or suggest a modification of Tanaka that that would remedy the deficiencies of Heim discussed above. In particular, Heim does not teach or suggest a semiconductor device that includes an insulating dielectric layer and a plurality of vias formed in an interlayer dielectric that is formed between a pad metal layer and a lower metal layer that has apertures, "wherein said interlayer dielectric covers a portion of both the bottom and the sides of said pad metal layer" and "wherein said insulating dielectric layer covers a portion of both the top and the sides of said pad metal layer" as is recited in Claim 1 (upon which Claims 3, 6 and 8 depend).

As understood by Applicants, Heim shows a bond pad scheme for semiconductor devices that is dissimilar to claimed embodiments of Applicants' invention. In particular,
passivation layer 218 which is equated in the outstanding Office Action to the recited insulating dielectric layer has significant differences thereto. Specifically, passivation layer 218 is not formed as the recited insulating dielectric layer is delimited in Claim 1 to be formed. More specifically, the passivation layer is shown as covering a portion of the top of conductive layer 214 and the entire sides of conductive layer (and not a portion of the sides thereof). In the embodiment set forth in Claim 1, only a portion of the sides of pad metal layer are covered by the recited insulating dielectric layer while the other portion of the sides of pad metal layer is covered by the recited interlayer dielectric layer. Accordingly, the subject matter that is referenced in the outstanding Office Action from Heim, cannot reasonably be considered to teach or suggest a modification of Tanaka that would remedy the deficiencies of Tanaka discussed above.

With regard to Claim 6, Applicants respectfully submit that nowhere in the Tanaka and Heim references is a semiconductor device that includes the above

discussed limitations of Claim 1 and further includes the limitations "wherein a probing process is performed on said center area of said pad metal layer" as is set forth in Claim 6 taught or suggested. With regard to Claim 7, Applicants respectfully submit that nowhere in the Tanaka and Heim references is a semiconductor device that includes the above discussed limitations of Claim 1 and further includes the limitations "wherein a wire-bonding process is performed on said center area of said pad metal layer" as is set forth in Claim 7 taught or suggested. With regard to Claim 8, Applicants respectfully submit that nowhere in the Tanaka and Heim references is a semiconductor device that includes the above discussed limitations of Claim 1 and further includes the limitations "wherein said semiconductor device is an integrated chip" as is set forth in Claim 8 taught or suggested.

Because of deficiencies of Tanaka and Heim discussed above, Applicants respectfully submit that Tanaka in view of Heim does not provide an adequate basis for rejection of Claim 1 under 35 U.S.C. §103 and, as such, Claim 1 is allowable. Accordingly, the Applicants respectfully submit that Claims 3 and 6-8 dependent on Claim 1 are likewise allowable as being dependent on allowable base claims (at least).

CONCLUSION

For at least the above-presented reasons, it is respectfully submitted that all remaining claims are in condition for allowance.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application. Please charge and additional fees or apply any credits to our PTO deposit account number: 50-4160

Respectfully submitted,
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